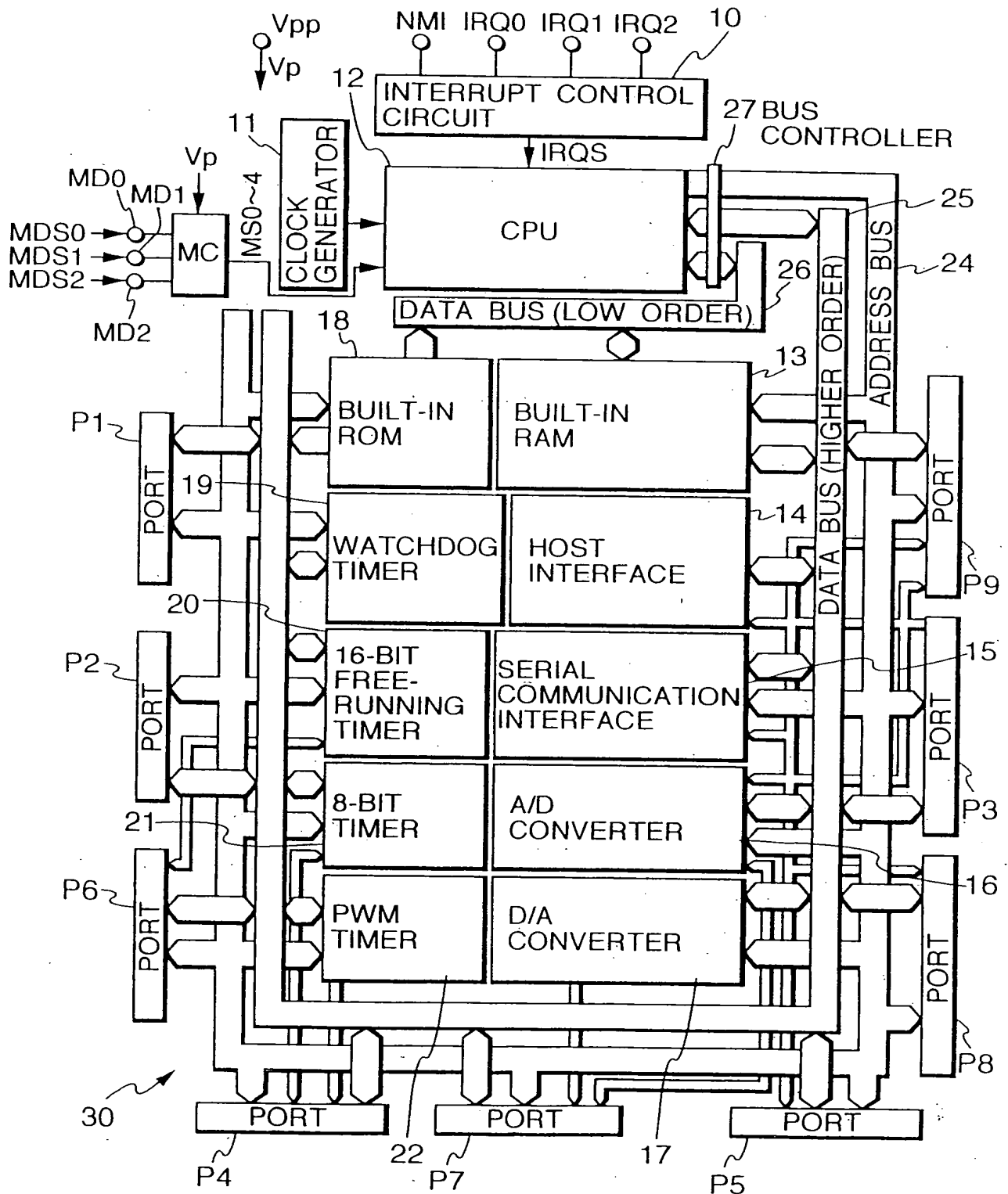


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FIG. 1



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FIG. 2

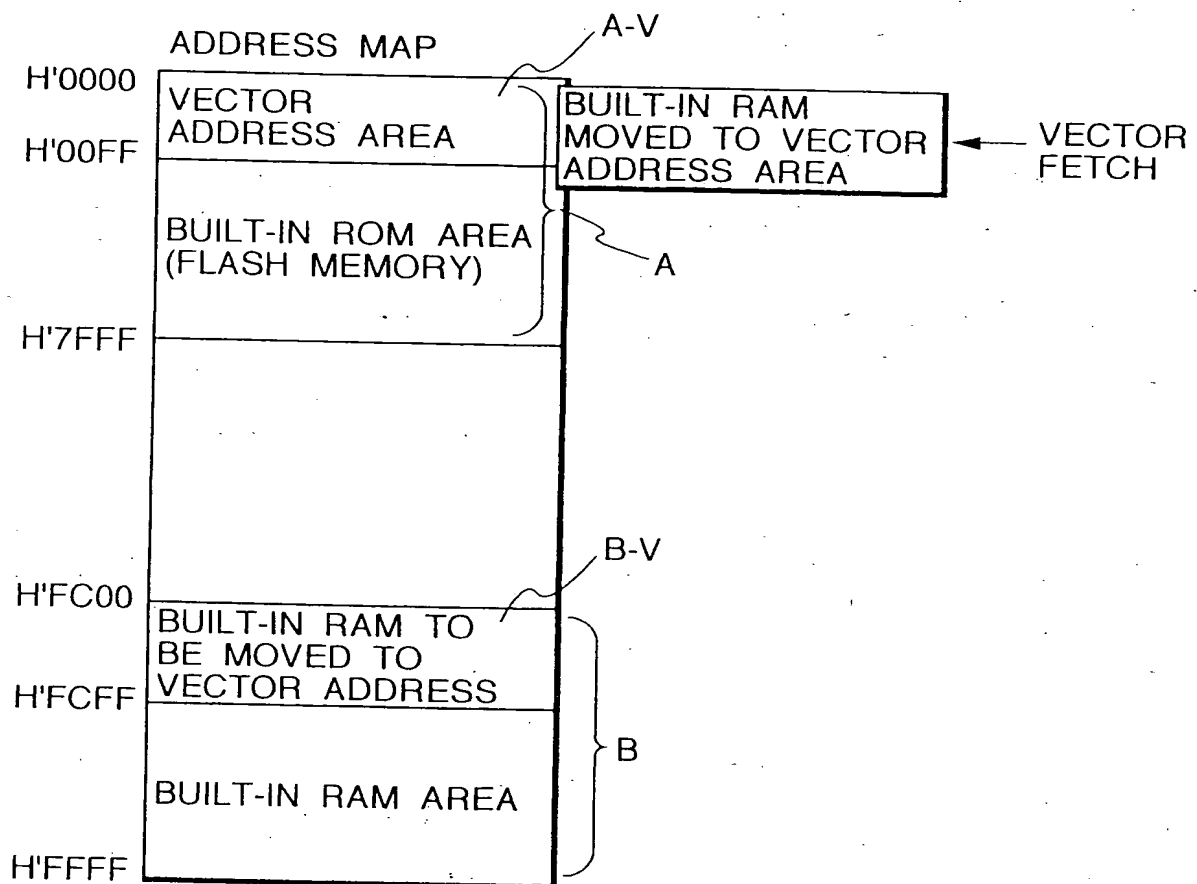
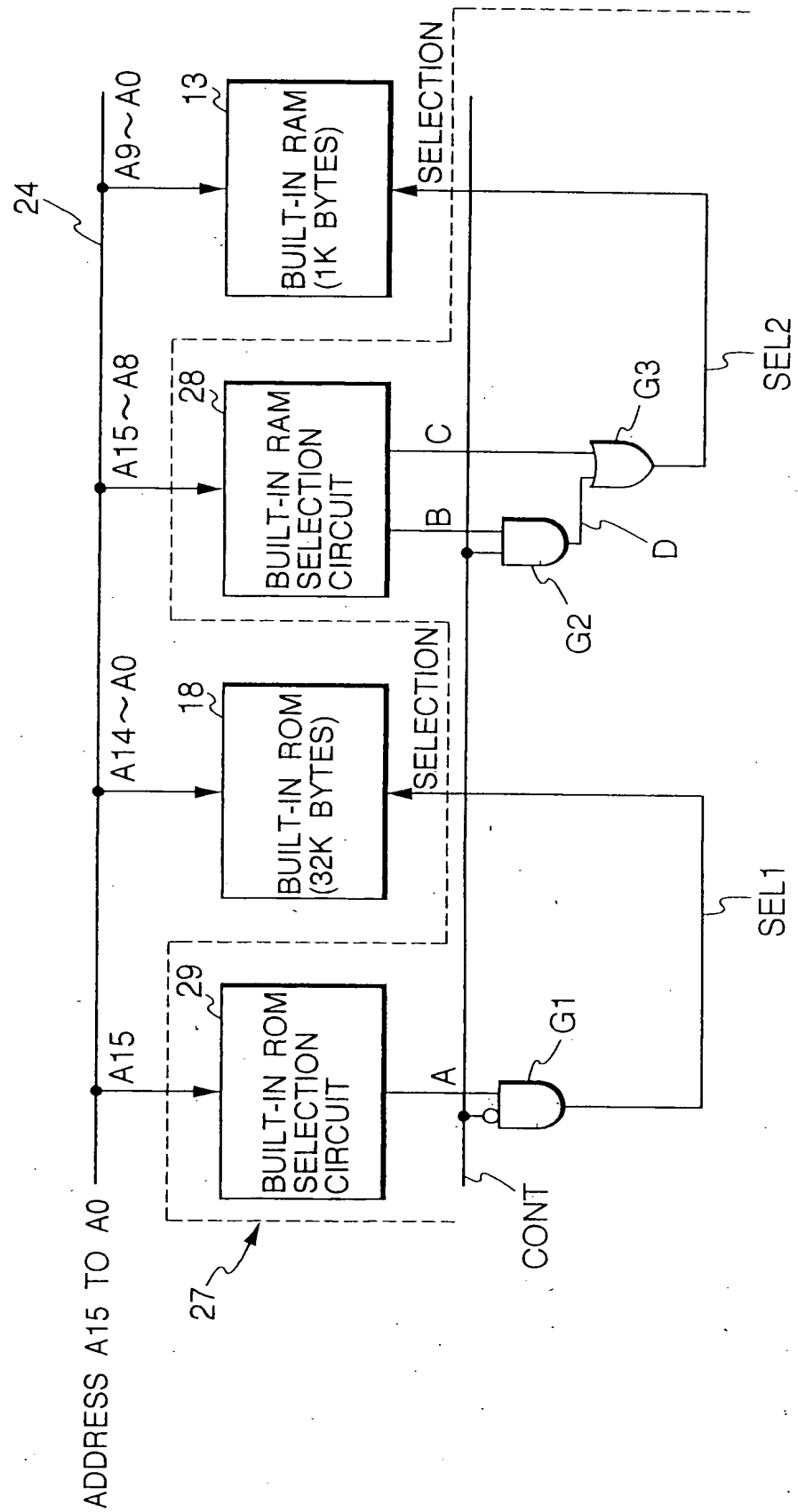
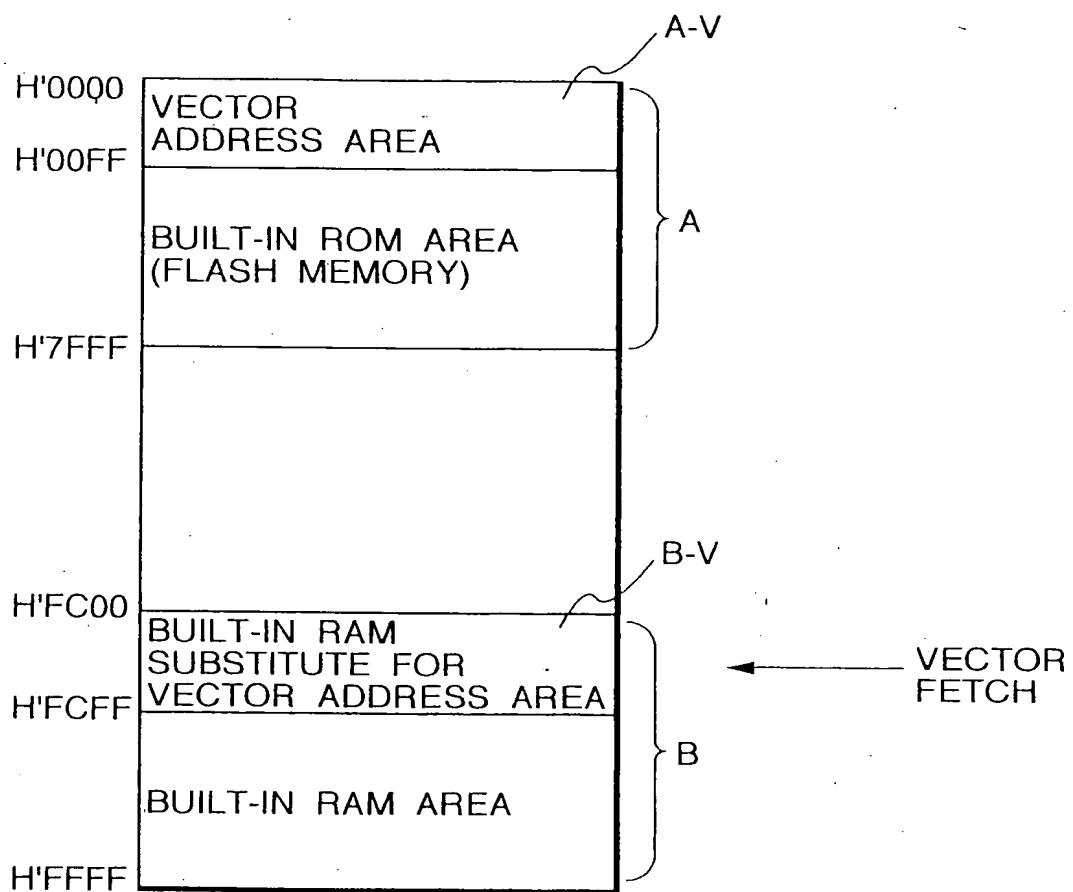


FIG. 3



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FIG. 4



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FIG. 5

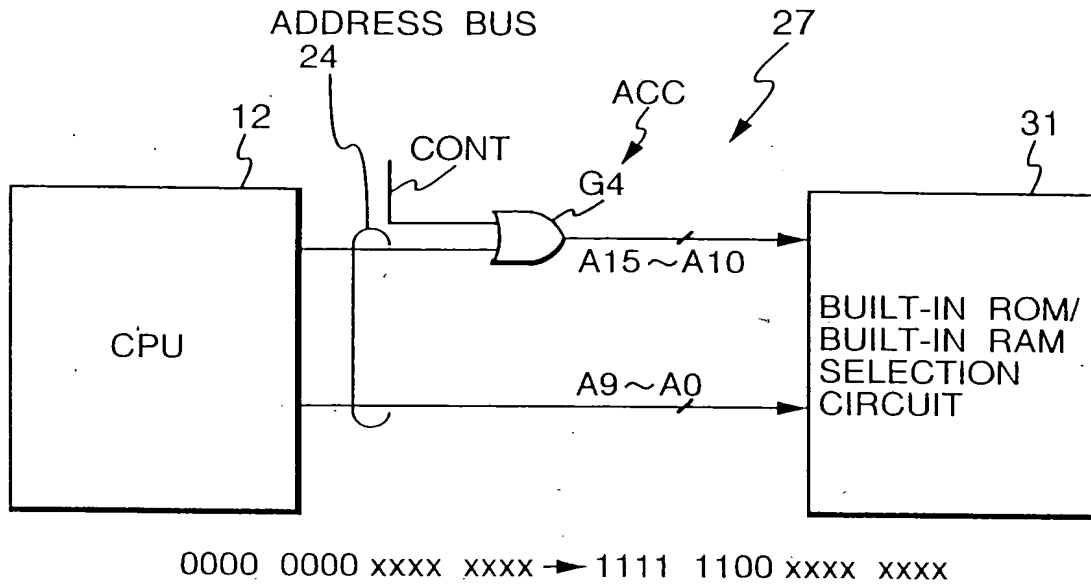
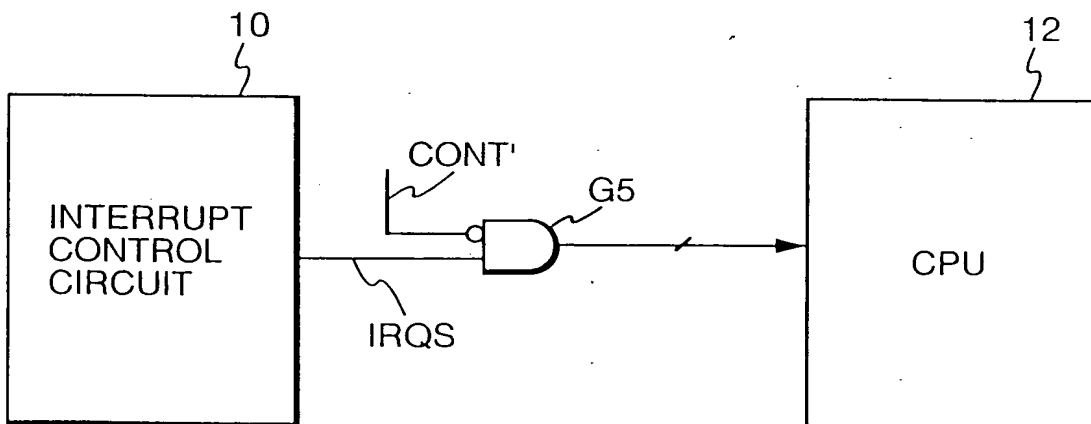


FIG. 6



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FIG. 7

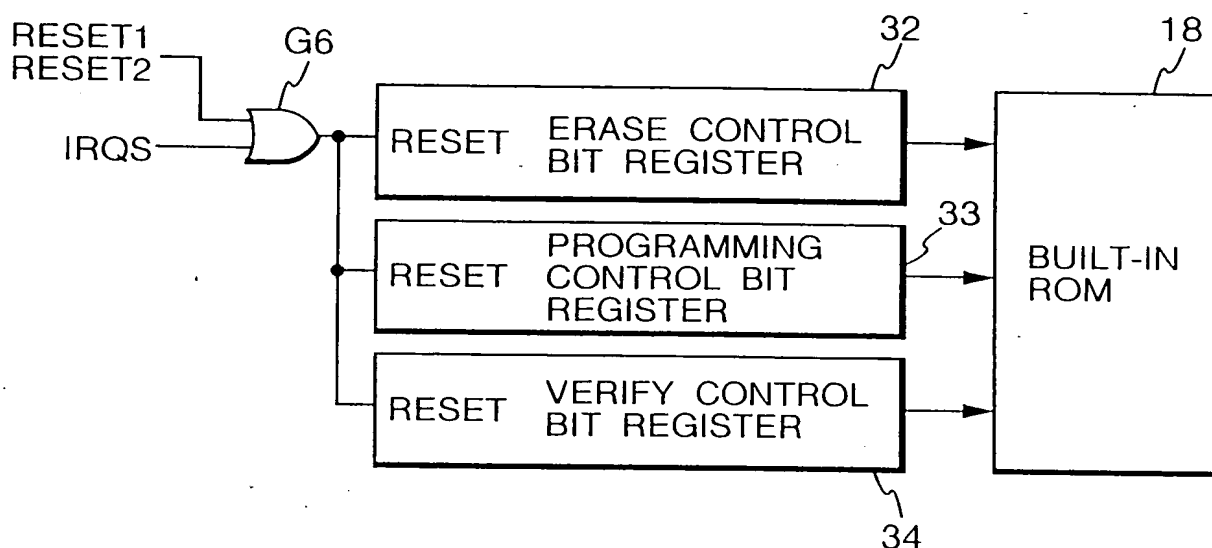
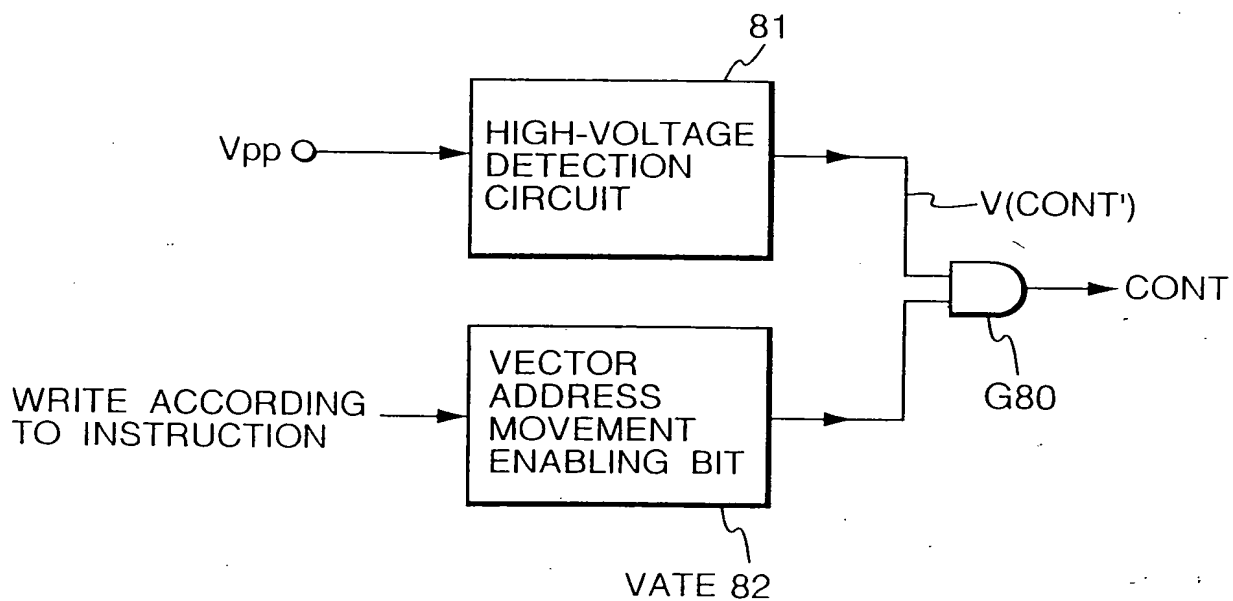
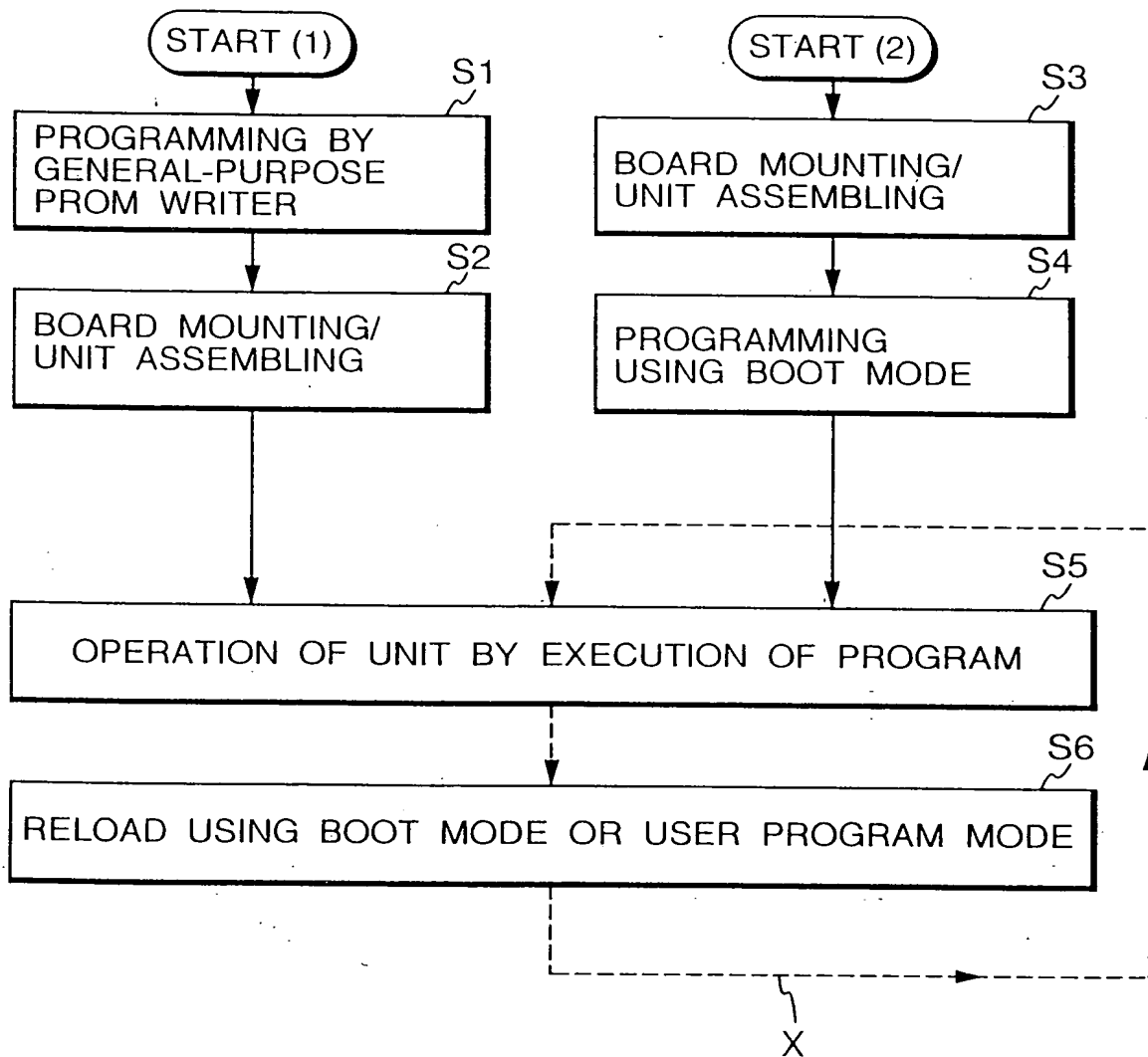


FIG. 8



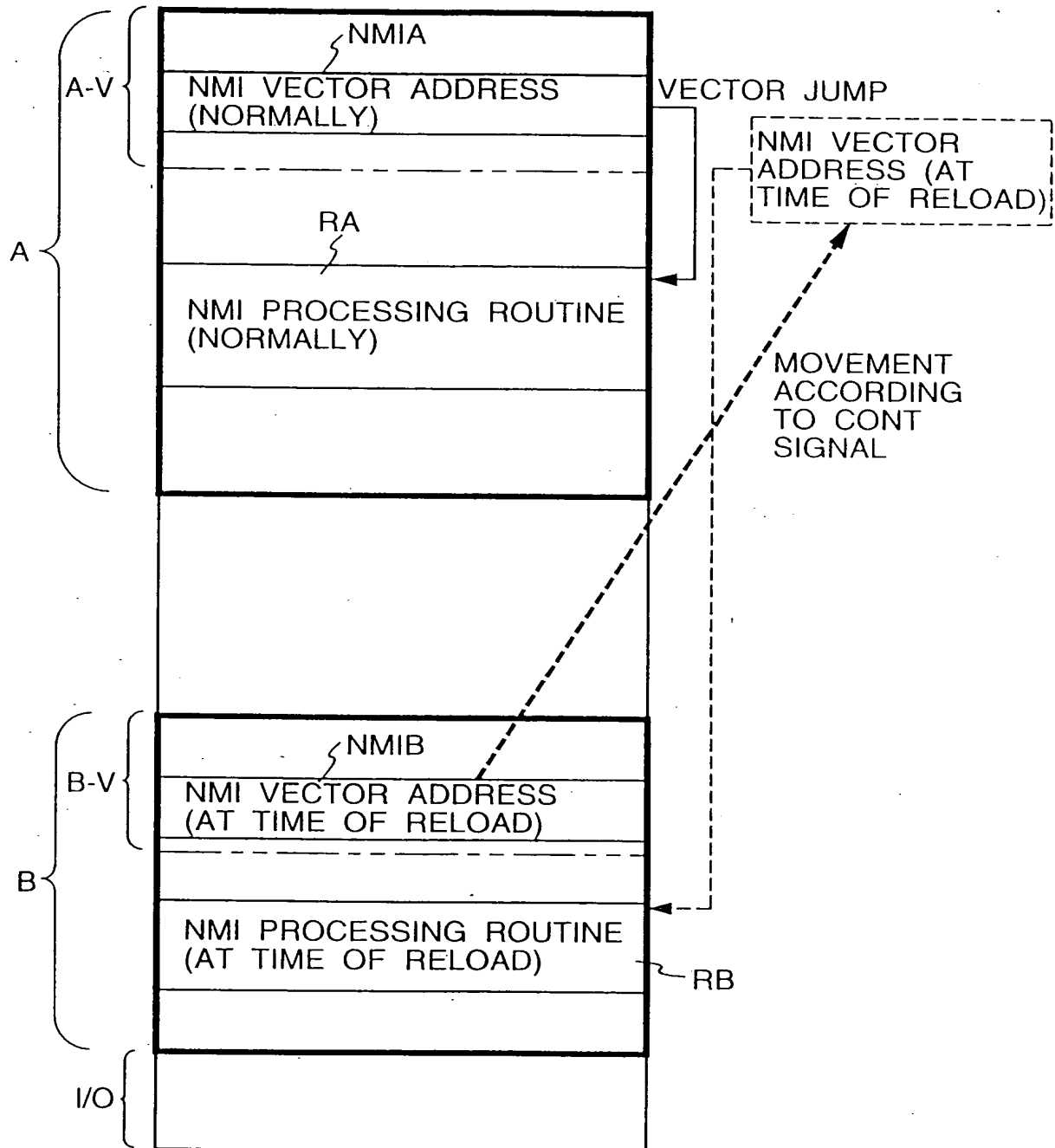
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FIG. 9



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FIG. 10



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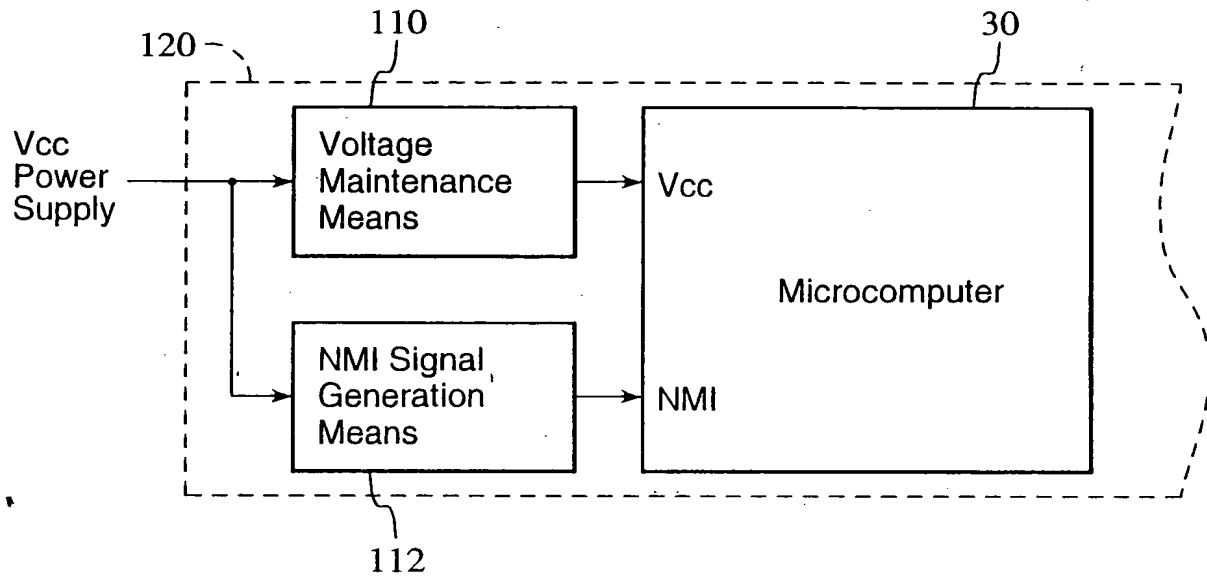


FIG. 11

PRINCIPLE OF FLASH MEMORY

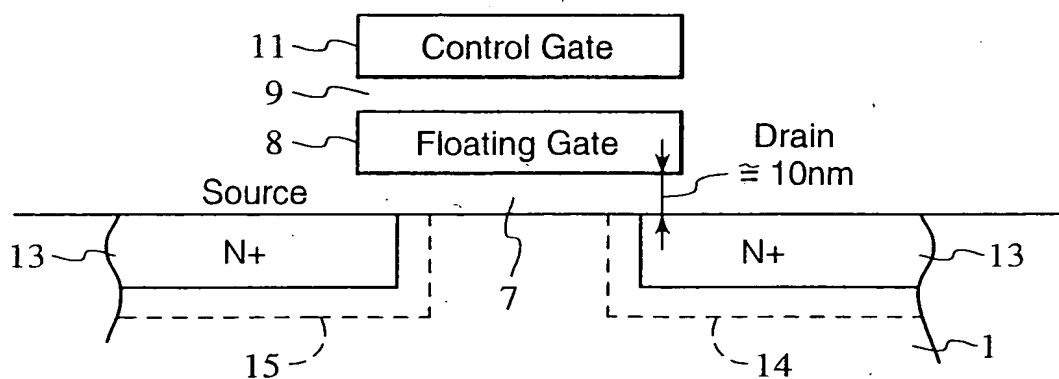
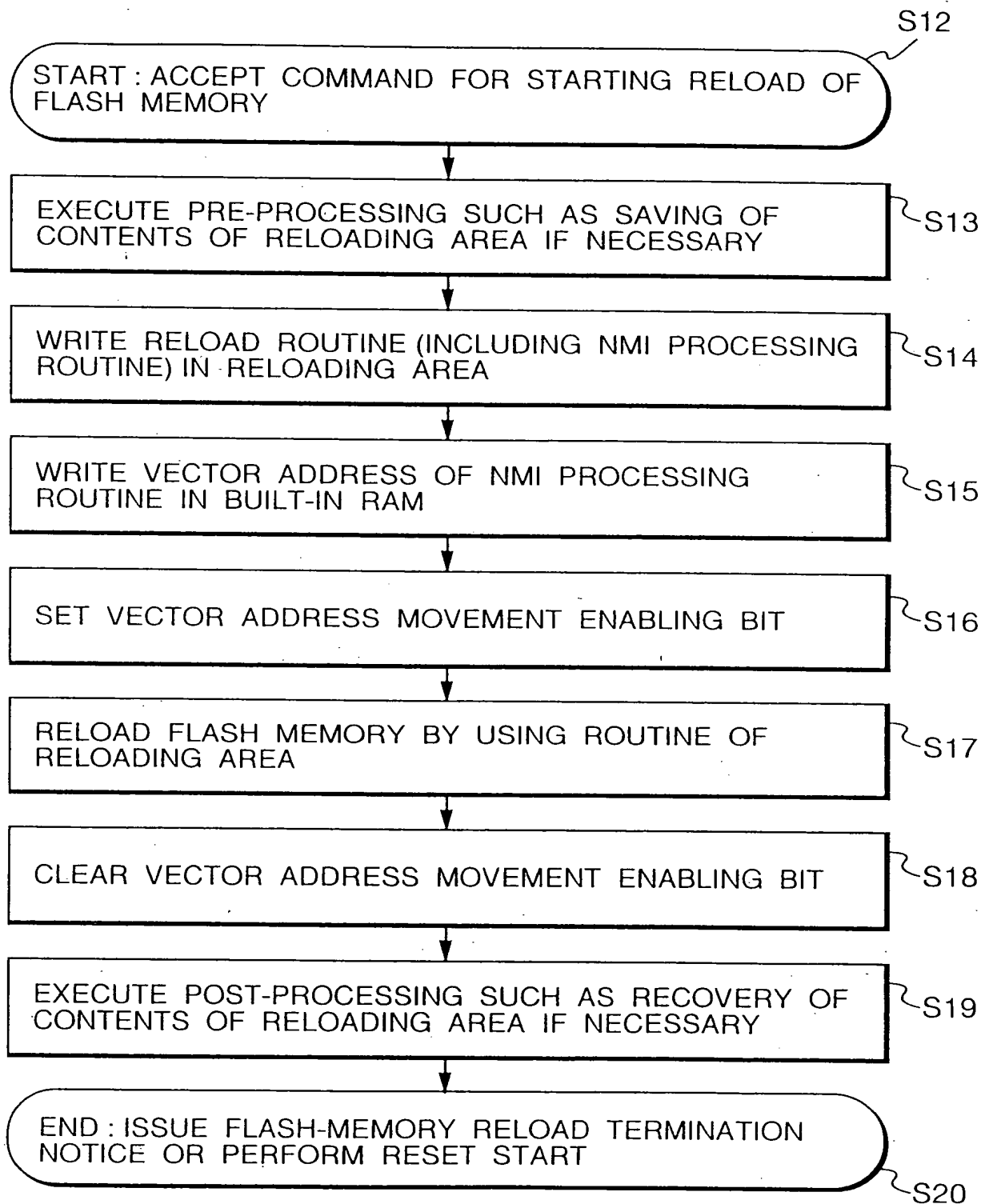


FIG. 13

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FIG. 12



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FIG. 14

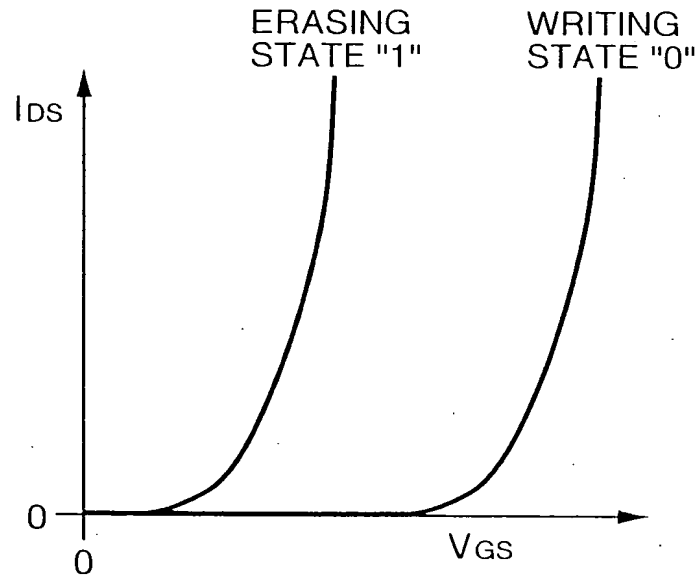
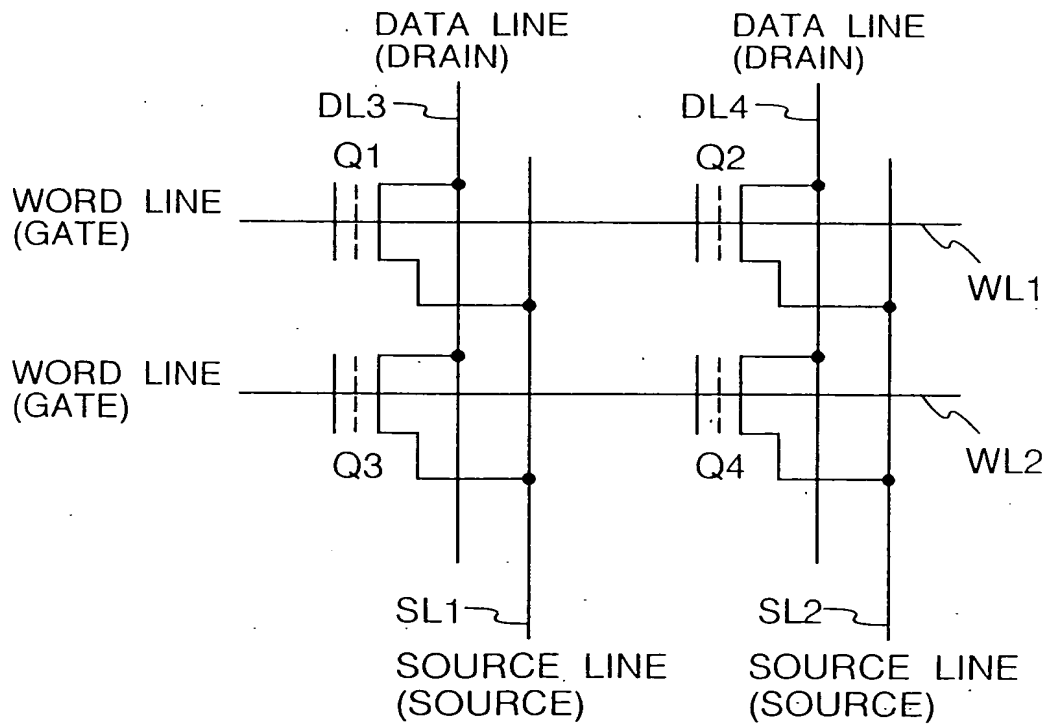


FIG. 15



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FIG. 16

WRITE

MEMORY DEVICE	SELECTIVE/ NON-SELECTIVE	SOURCE	DRAIN	GATE
Q1	SELECTIVE	0v	6v	12v
Q2	NON-SELECTIVE	0v	0v	12v
Q3	NON-SELECTIVE	0v	6v	0v
Q4	NON-SELECTIVE	0v	0v	0v

ERASE (POSITIVE VOLTAGE SYSTEM)

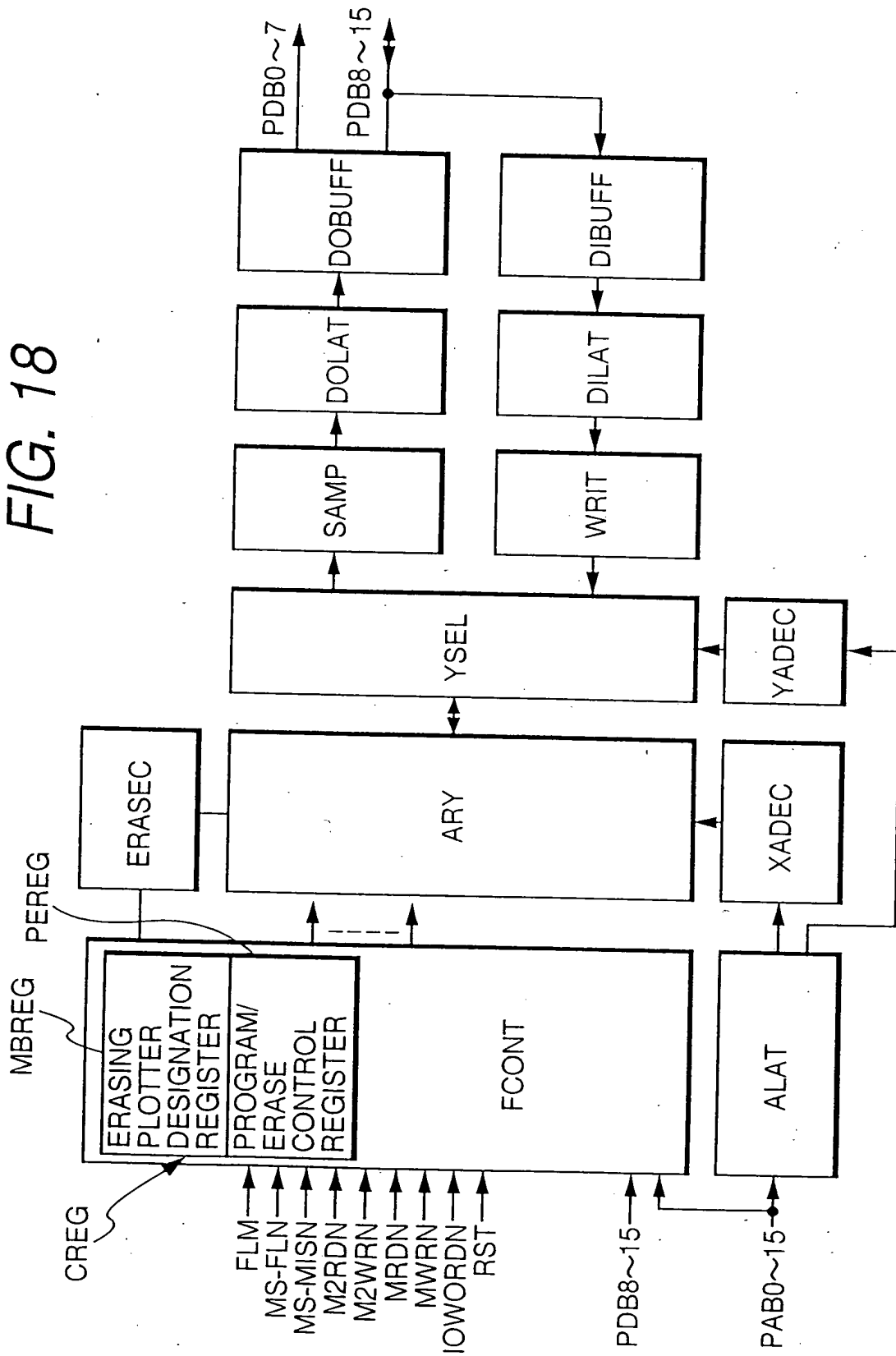
MEMORY DEVICE	SELECTIVE/ NON-SELECTIVE	SOURCE	DRAIN	GATE
Q1,Q3	SELECTIVE	12v	0v	0v
Q2,Q4	NON-SELECTIVE	0v	0v	0v

ERASE (NEGATIVE VOLTAGE SYSTEM)

MEMORY DEVICE	SELECTIVE/ NON-SELECTIVE	SOURCE	DRAIN	GATE
Q1,Q2	SELECTIVE	5v	0v	10v
Q3,Q4	NON-SELECTIVE	5v	0v	0v

The diagram illustrates the internal structure of the 18(FMRY) memory array. It features a central array of memory cells organized in rows and columns. The rows are controlled by word lines (WL0 to WLn) and the columns by bit lines (DL0 to DL7). The array is surrounded by control logic blocks including XALAT, XADEC, YALAT, YADEC, WE CONT, WRIT DILAT, and SAMP. The output of the array is connected to the DOBUFF and DOBUFF blocks. The array is also connected to the 18(FMRY) memory array and the 18(FMRY) memory array.

FIG. 18



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FIG. 19

CONTROL REGISTER

PROGRAM / ERASE CONTROL REGISTER

Vpp				EV	PV	E	P
-----	--	--	--	----	----	---	---

PEREG

MBREG1

ERASING BLOCK DESIGNATION REGISTER

	6	5	4	3	2	1	0
--	---	---	---	---	---	---	---

MBREG2

ERASING BLOCK DESIGNATION REGISTER

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

Vpp : Vpp APPLYING FLAG

E : ERASE
P : PROGRAM

EV : ERASE VERIFY
PV : PROGRAM VERIFY

MBREG1 : FOR DESIGNATION OF LARGE BLOCK
MBREG2 : FOR DESIGNATION OF SMALL BLOCK